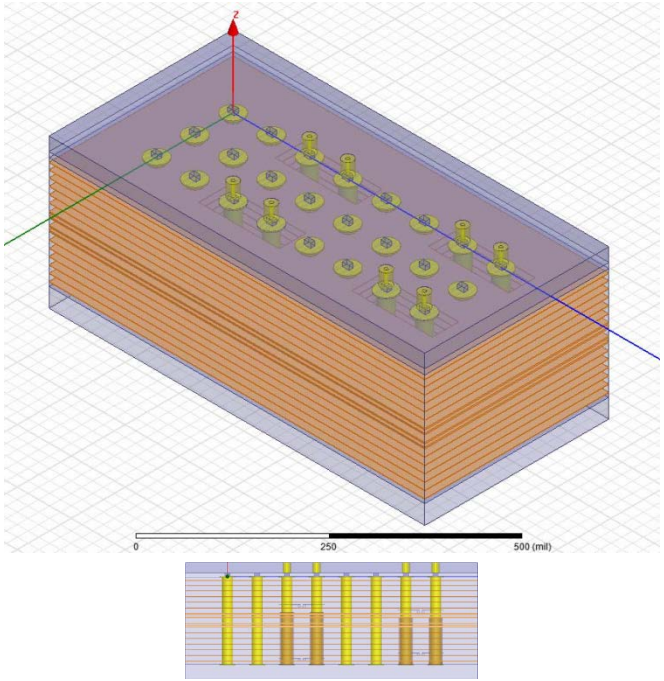
Signal integrity & simulation considerations in VPX backplane designs

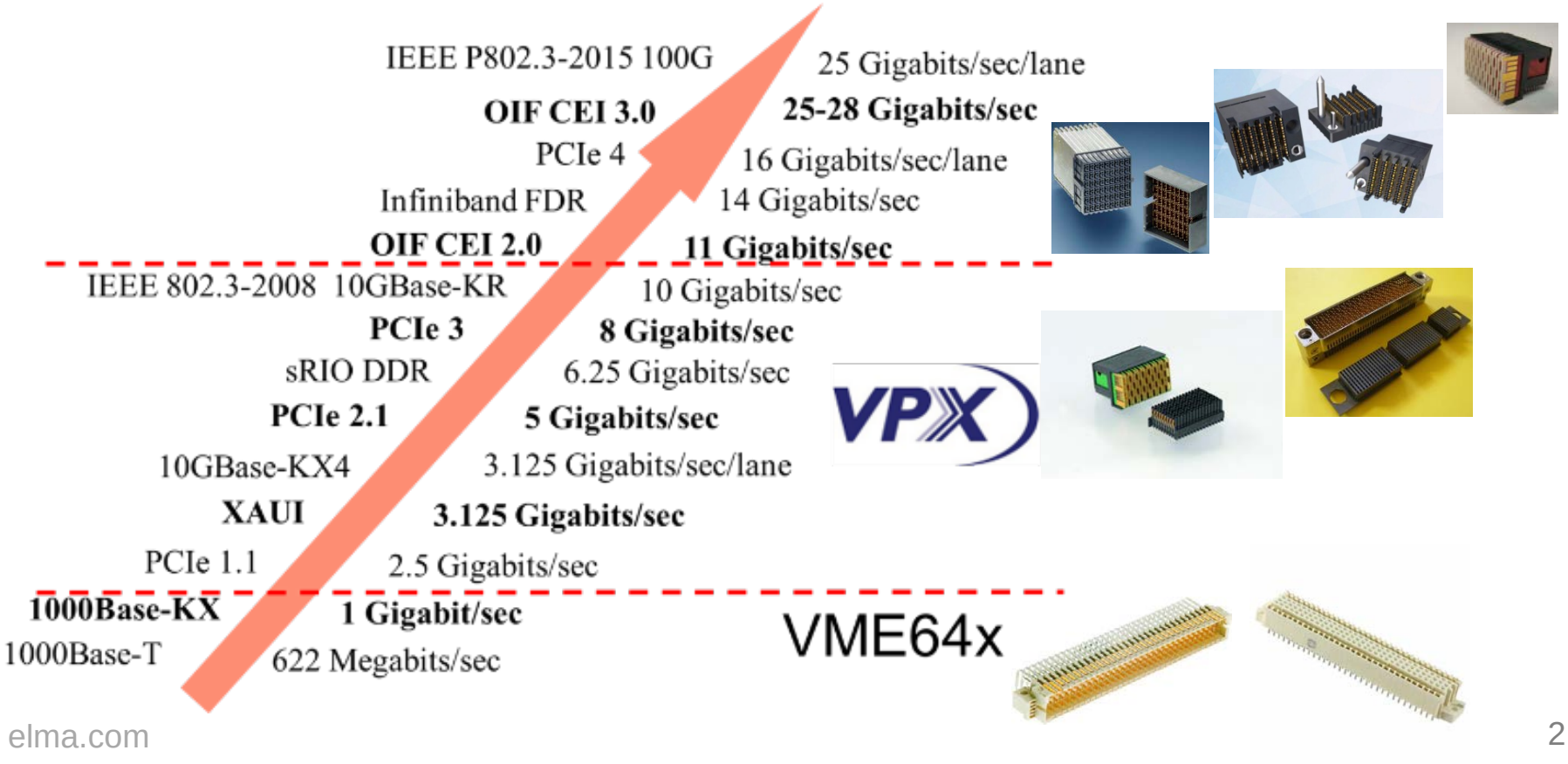


Ovidiu Mesesan

Embedded Tech Trends, Jan 22-23

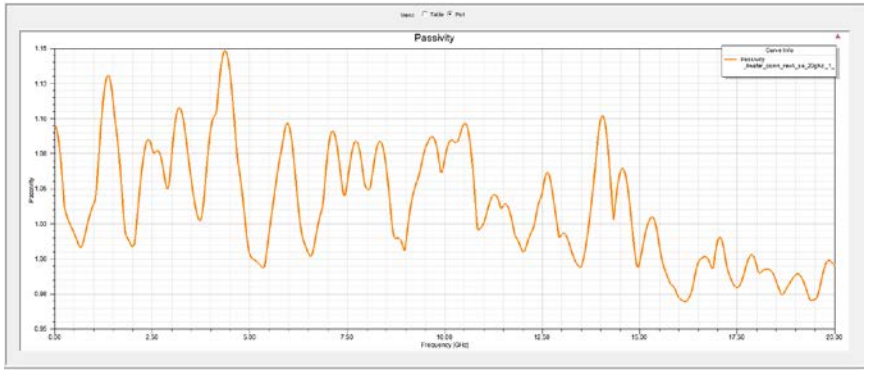
Connectorization & standardization

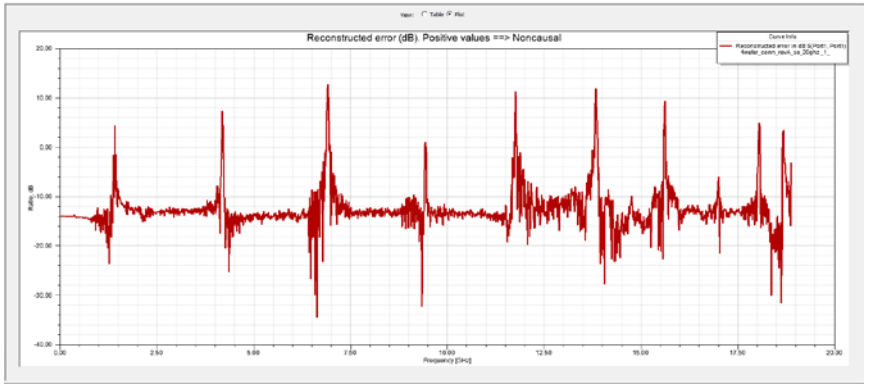
Advances and challenges in connector technology

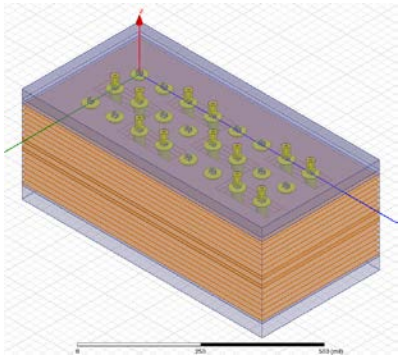


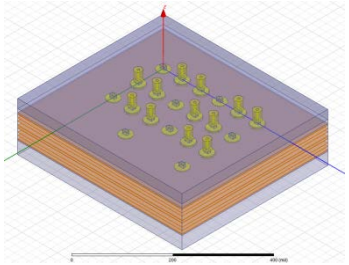
Connector issues

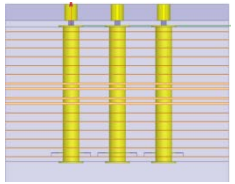
Passivity, causality, footprints design & optimization

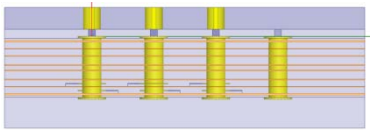






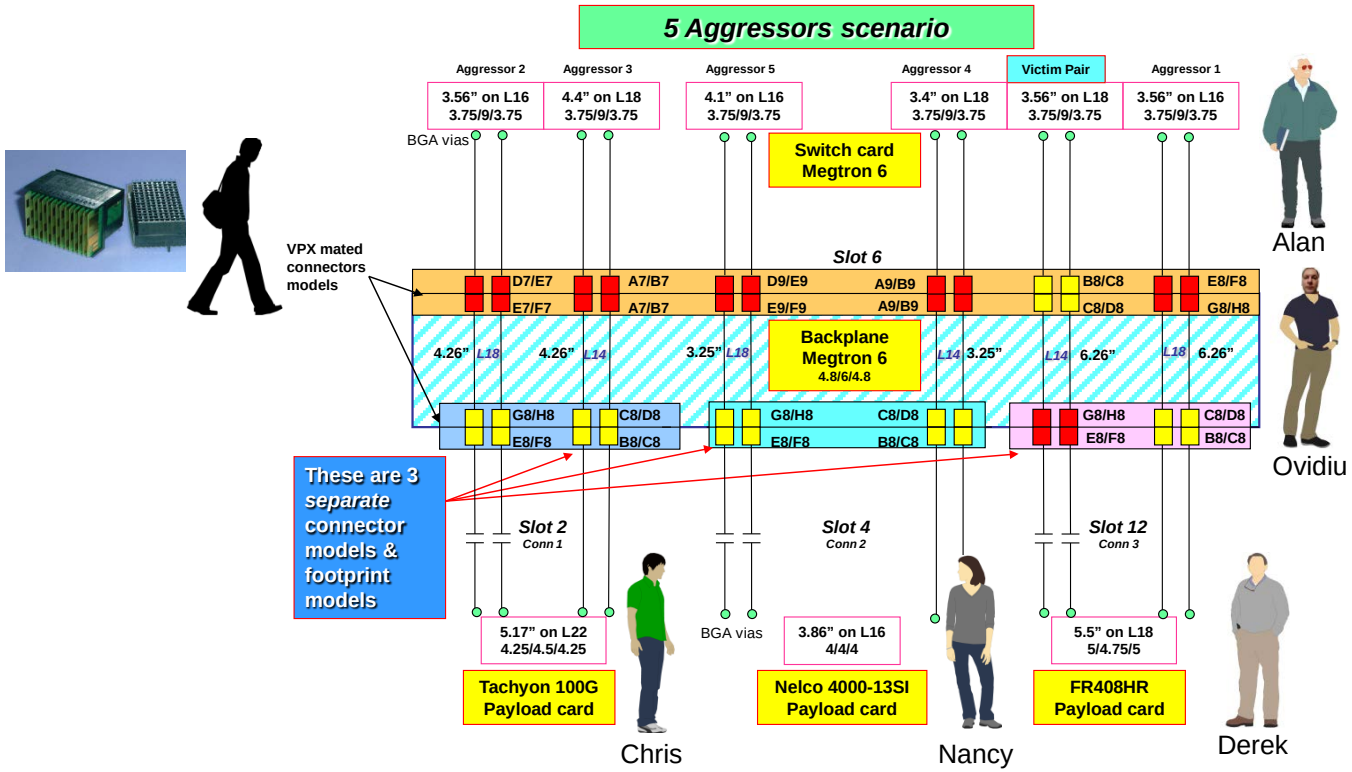






Channel simulation & design

Connectors as part of the channel model



S-parameters

S-parameters cascading issues (the good, the bad and the ugly)

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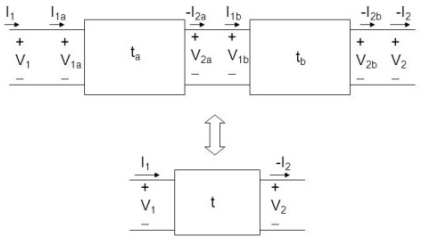
THE GOOD

TWO-PORT NETWORK

Interconnection of networks

Cascade: t parameters



$[t] = [t_a][t_b]$

Scattering transfer parameters

$$S_{11} = \frac{T_{21}}{T_{11}}$$

$$S_{12} = \frac{T_{11}T_{22} - T_{12}T_{21}}{T_{11}}$$

$$S_{21} = \frac{1}{T_{11}}$$

$$S_{22} = \frac{-T_{12}}{T_{11}}$$

THE BAD

πάντων γὰρ ὅσα πλείω μέρη ἔχει καὶ μὴ ἔστιν οἷον σωρὸς τὸ πᾶν

(Αριστοτέλης, "Τὰ μετὰ τὰ φυσικά", cca 330 BCE)

The totality is not, as it were, a mere heap, but the whole is something besides the parts.

(Aristotle, "Metaphysics", Book VIII, 1045a.9)

THE UGLY

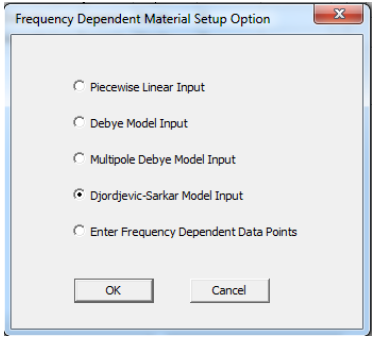
Cascaded S-parameters are NOT a physical reality

(Heidi Barnes, cca 2008 CE)

Channel simulation

Simulations assumptions

A simulation can only be as good as the models and assumptions that are being used in the process!



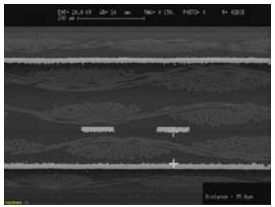
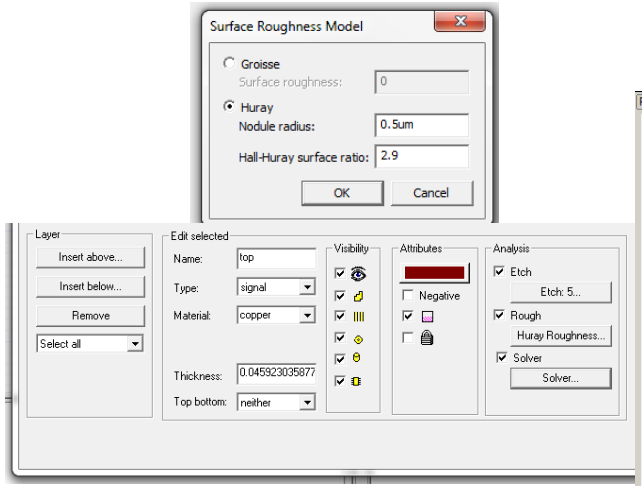


Image courtesy of Polar Instruments (Spur Electron Limited, Havant, Hampshire, UK)



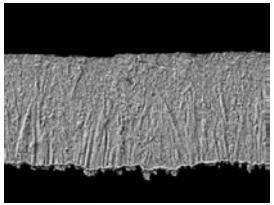
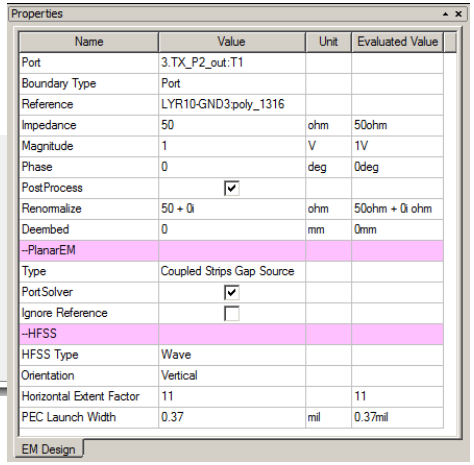
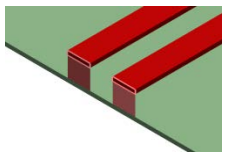
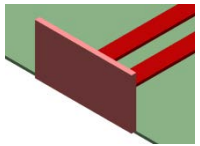


Image courtesy of Taconic Advanced Dielectric Division



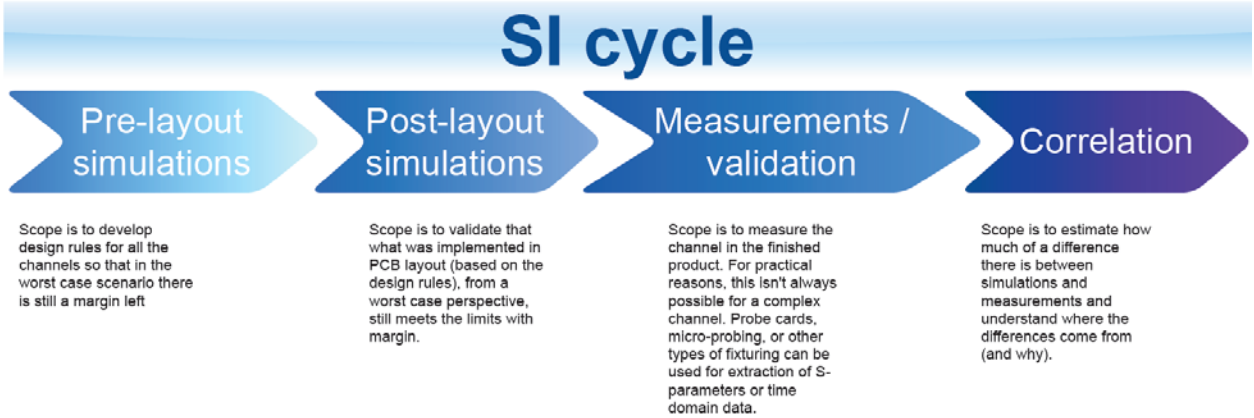
Name	Value	Unit	Evaluated Value
Port	3.TX_P2_out:T1		
Boundary Type	Port		
Reference	LYR10-GND3:poly_1316		
Impedance	50	ohm	50ohm
Magnitude	1	V	1V
Phase	0	deg	0deg
PostProcess	☑		
Renormalize	50 + 0i	ohm	50ohm + 0i ohm
Deembed	0	mm	0mm
--PlanarEM			
Type	Coupled Strips Gap Source		
PortSolver	☑		
Ignore Reference	☐		
--HFSS			
HFSS Type	Wave		
Orientation	Vertical		
Horizontal Extent Factor	11		11
PEC Launch Width	0.37	mil	0.37mil

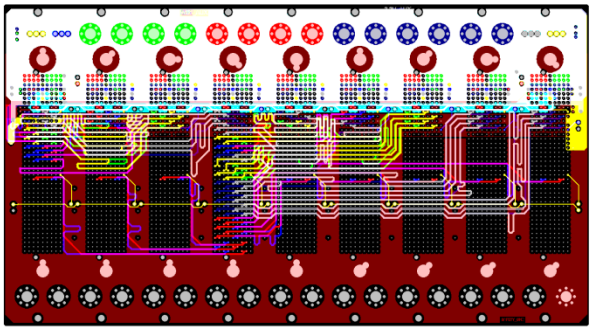


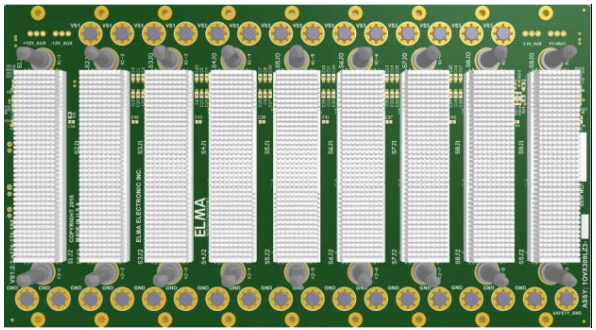


Channel design

SI flow

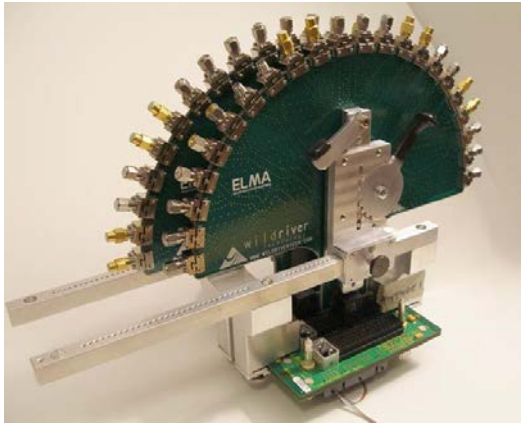


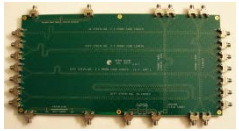


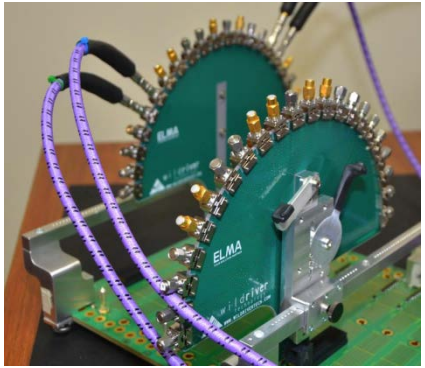


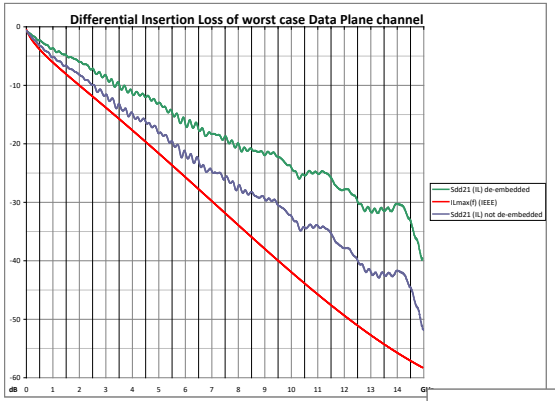
Backplane channel measurements

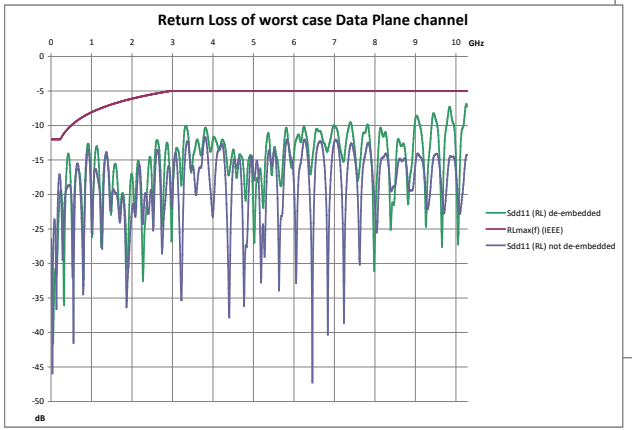
Measurements and why good launches are necessary

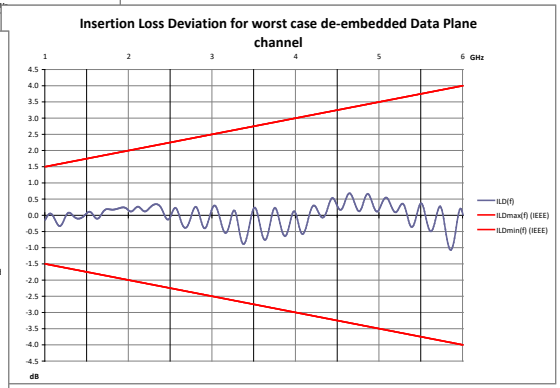












Channel co-design (& co-simulation!)

(or “Why Nancy, Alan, Derek, Chris & Ovidiu shouldn’t have a Mexican standoff”)

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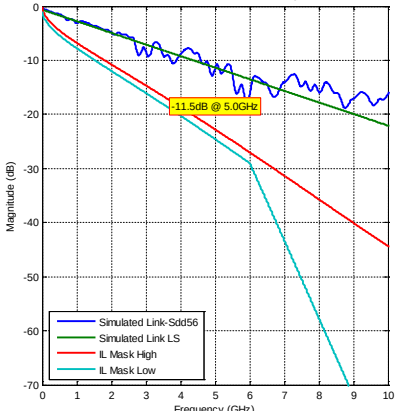
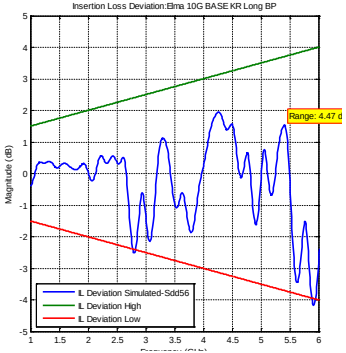
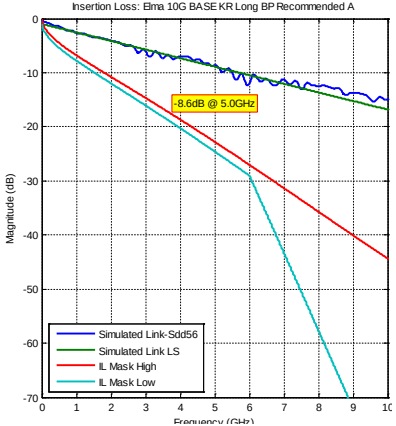
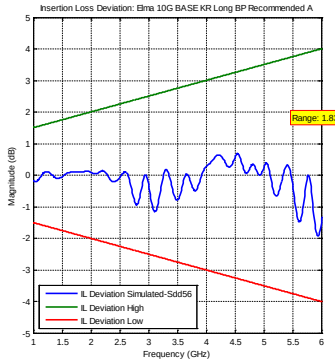
Derek’s existing design

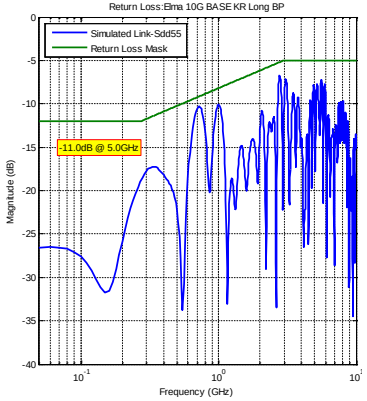


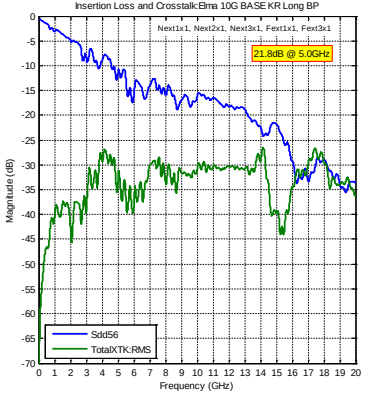


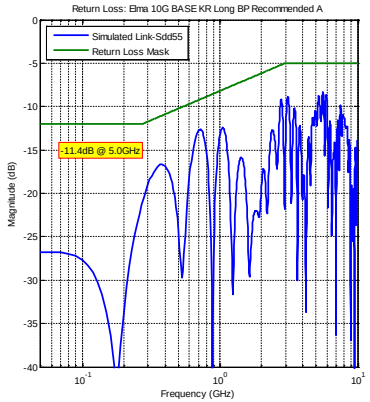
Derek’s improved design

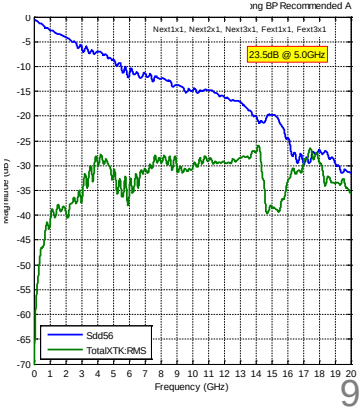






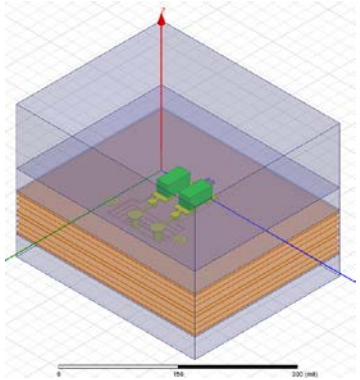


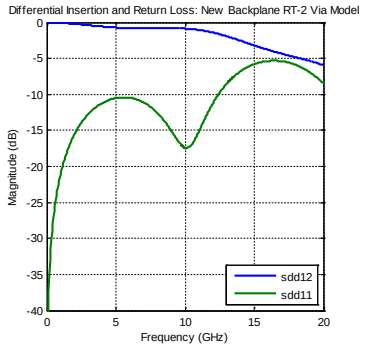


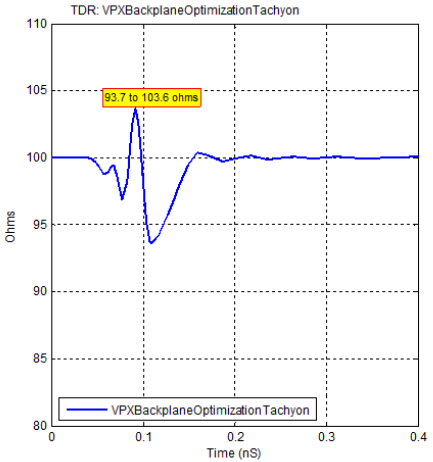


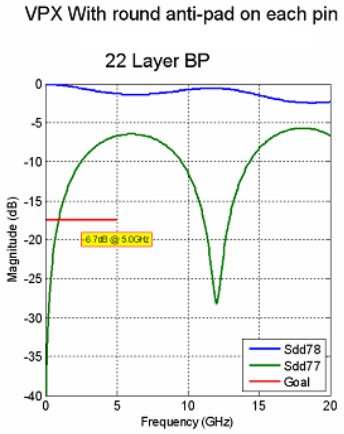
Channel co-design

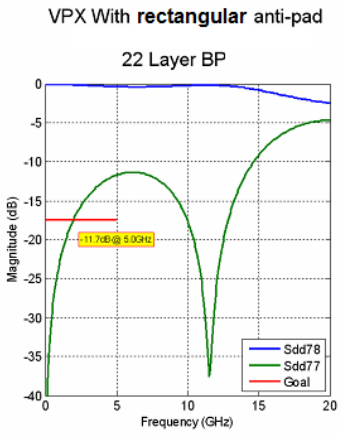
Improvements – vias on daughtercards and backplane

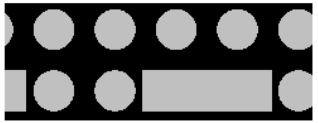












Channel co-design

Improvements for a common goal

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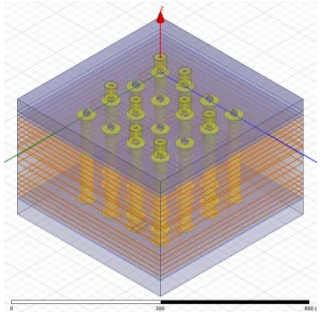

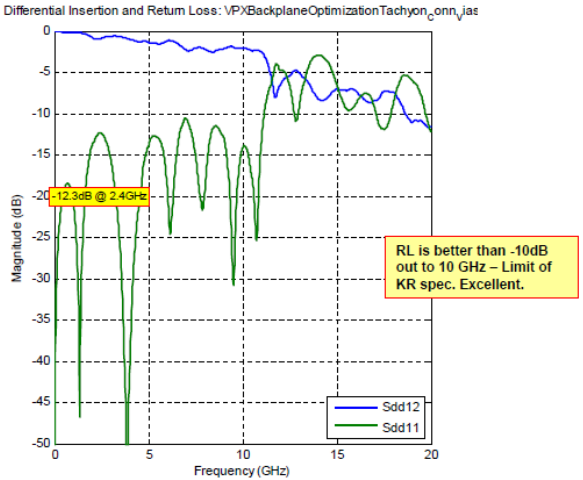

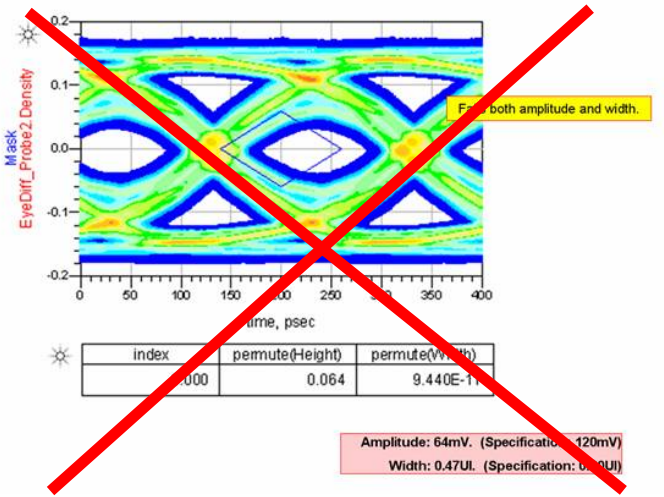

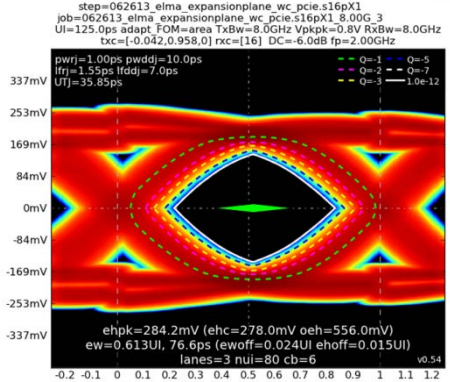

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- **Questions?**

- **Thank you for your time!**

- Ovidiu Mesesan
- Embedded Tech Trends 2018 Austin, Texas