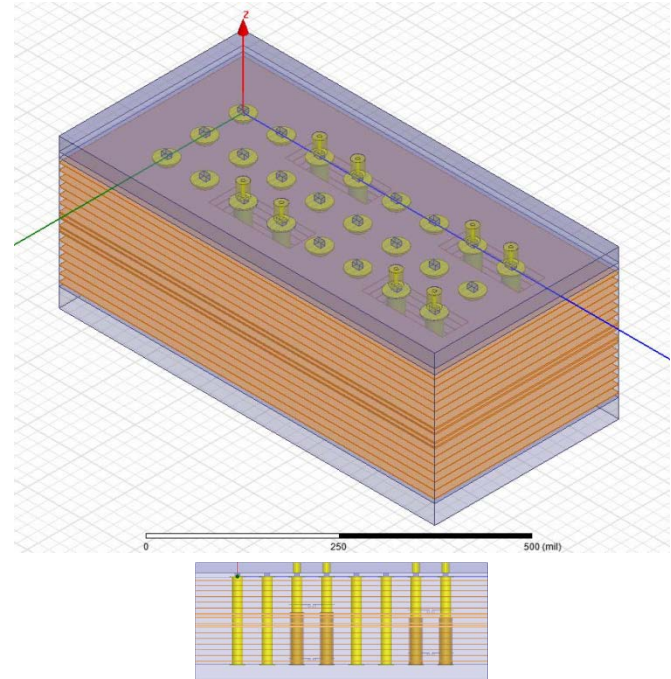


Signal integrity & simulation considerations in VPX backplane designs

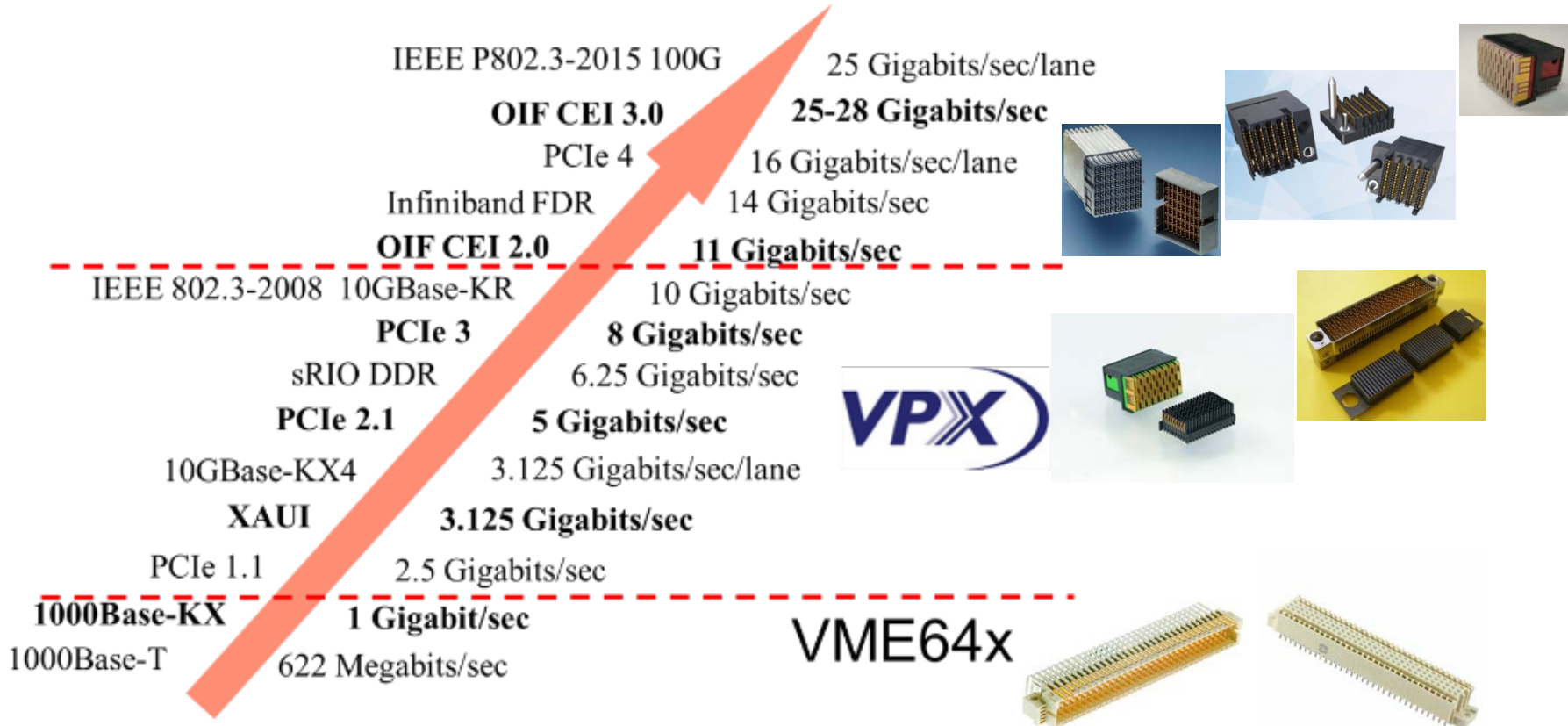
Ovidiu Mesezan

Embedded Tech Trends, Jan 22-23



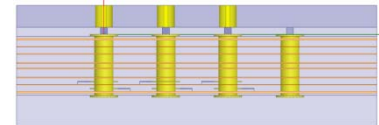
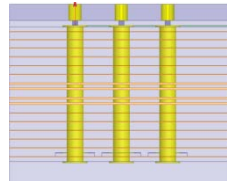
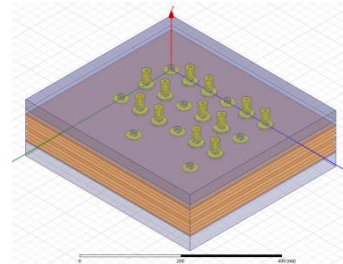
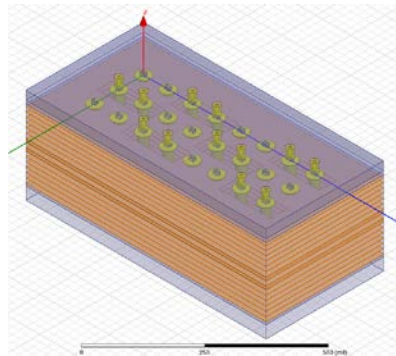
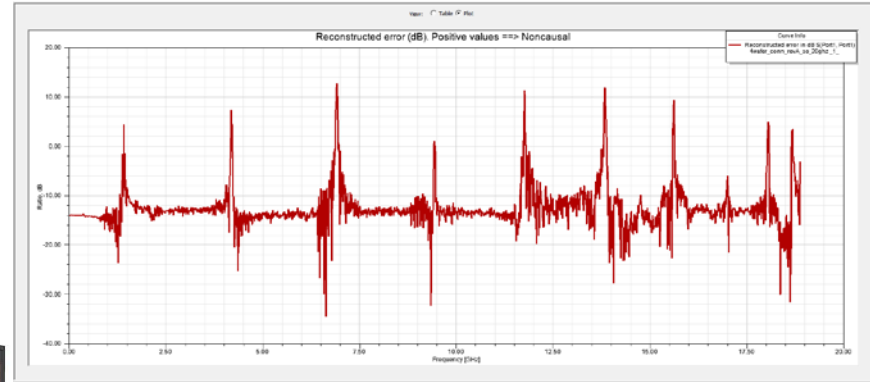
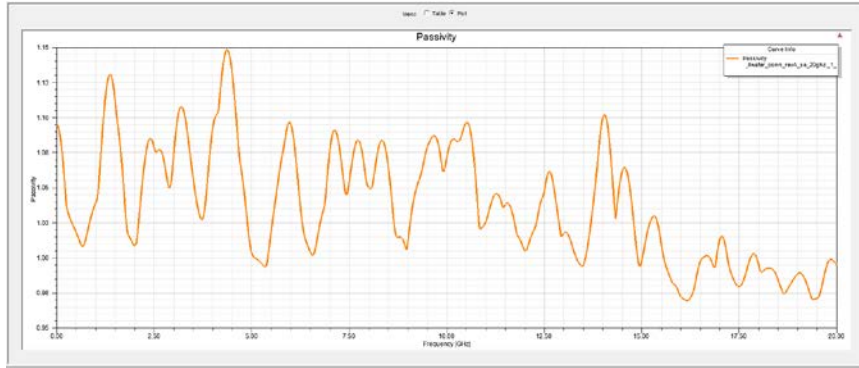
Connectorization & standardization

Advances and challenges in connector technology



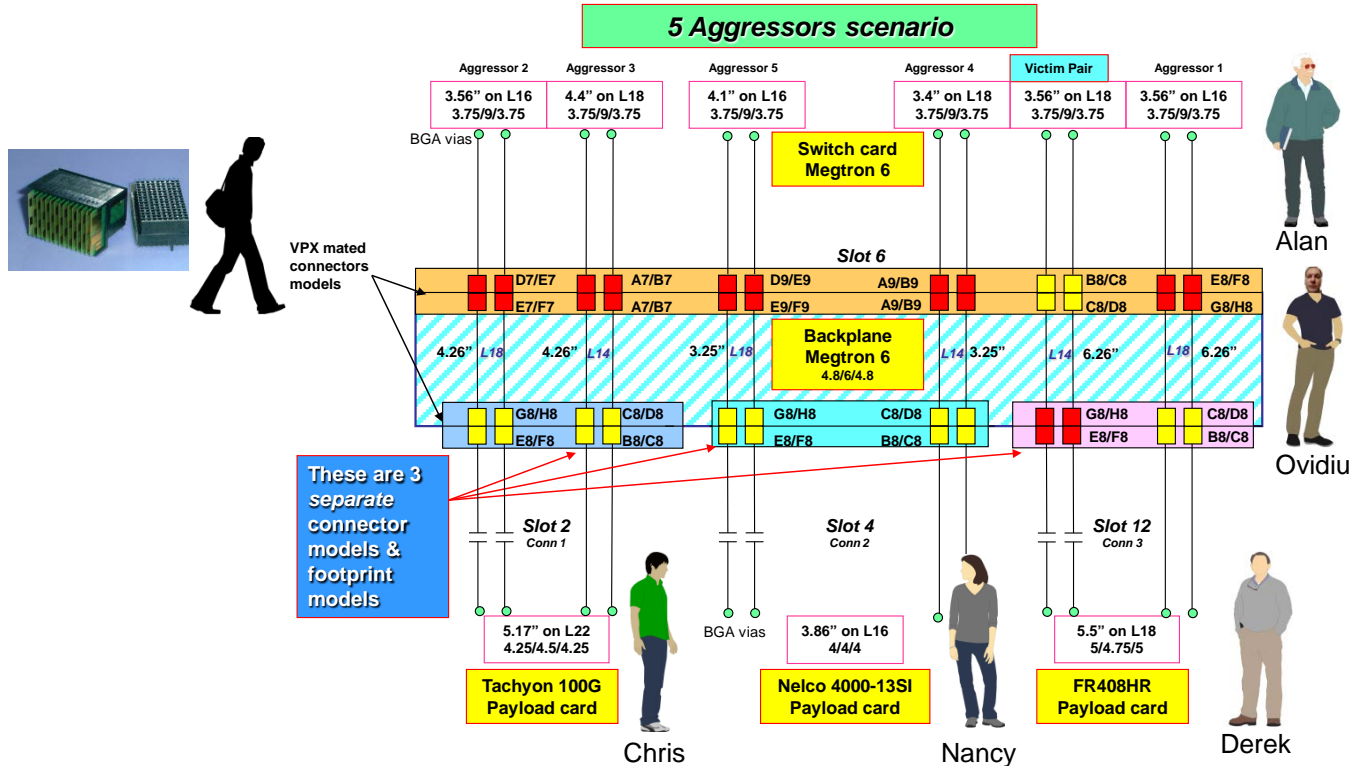
Connector issues

Passivity, causality, footprints design & optimization



Channel simulation & design

Connectors as part of the channel model



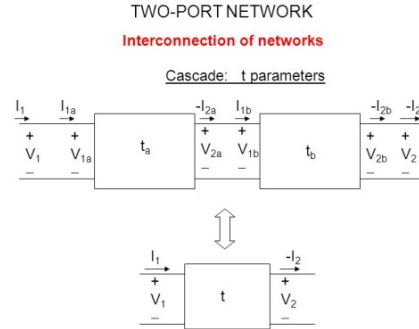
S-parameters

S-parameters cascading issues (the good, the bad and the ugly)

THE GOOD



Everybody's doing it!



Scattering transfer parameters

$$S_{11} = \frac{T_{21}}{T_{11}}$$

$$S_{12} = \frac{T_{11}T_{22} - T_{12}T_{21}}{T_{11}}$$

$$S_{21} = \frac{1}{T_{11}}$$

$$S_{22} = \frac{-T_{12}}{T_{11}}$$

THE BAD

πάντων γὰρ ὅσα πλείω μέρη ἔχει καὶ μὴ ἔστιν οἶον σωρὸς τὸ πᾶν

(Aristotle, "Τὰ μετὰ τὰ φυσικά", cca 330 BCE)

The totality is not, as it were, a mere heap, but the whole is something besides the parts.

(Aristotle, "Metaphysics", Book VIII, 1045a.9)



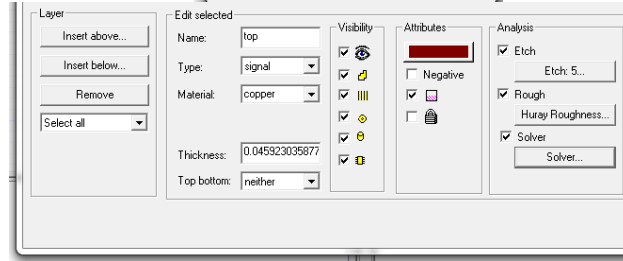
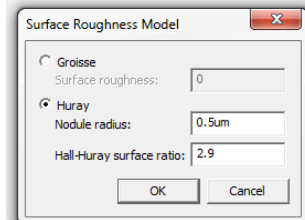
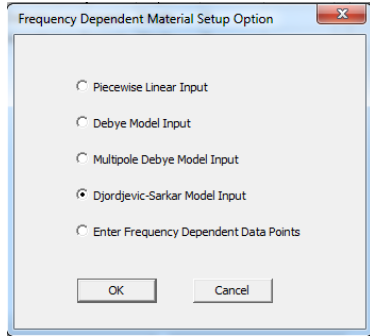
THE UGLY

Cascaded S-parameters are
• NOT a physical reality •

(Heidi Barnes, cca 2008 CE)

Simulations assumptions

A simulation can only be as good as the models and assumptions that are being used in the process!



Properties

Name	Value	Unit	Evaluated Value
Port	3.TX_P2_out.T1		
Boundary Type	Port		
Reference	LYR10-GND3.poly_1316		
Impedance	50	ohm	50ohm
Magnitude	1	V	1V
Phase	0	deg	0deg
PostProcess	<input checked="" type="checkbox"/>		
Renormalize	50 + 0i	ohm	50ohm + 0i ohm
Deembed	0	mm	0mm
-PlanarEM			
Type	Coupled Strips Gap Source		
PortSolver	<input checked="" type="checkbox"/>		
Ignore Reference	<input type="checkbox"/>		
-HFSS			
HFSS Type	Wave		
Orientation	Vertical		
Horizontal Extent Factor	11		11
PEC Launch Width	0.37	mil	0.37mil

EM Design

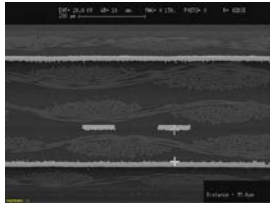


Image courtesy of Polar Instruments (Spur Electron Limited, Havant, Hampshire, UK)

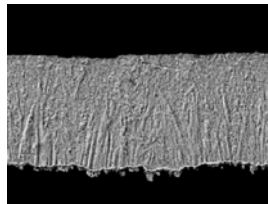
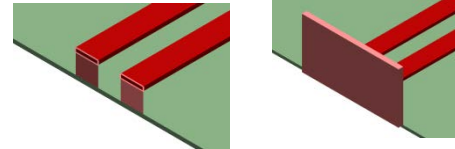


Image courtesy of Taconic Advanced Dielectric Division



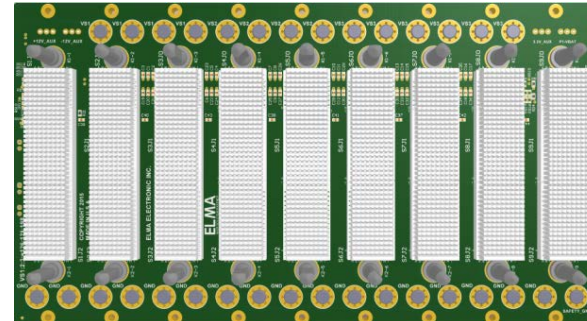
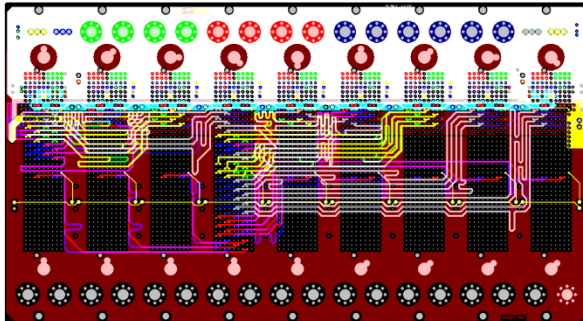


Scope is to develop design rules for all the channels so that in the worst case scenario there is still a margin left

Scope is to validate that what was implemented in PCB layout (based on the design rules), from a worst case perspective, still meets the limits with margin.

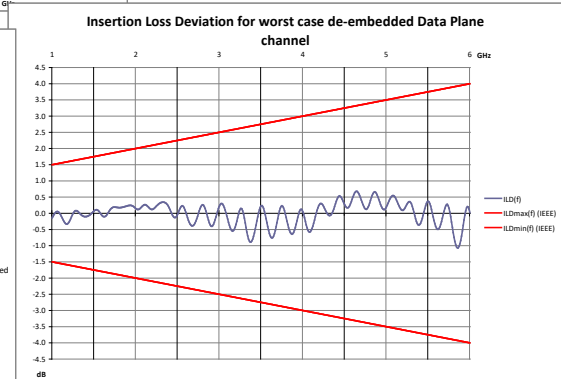
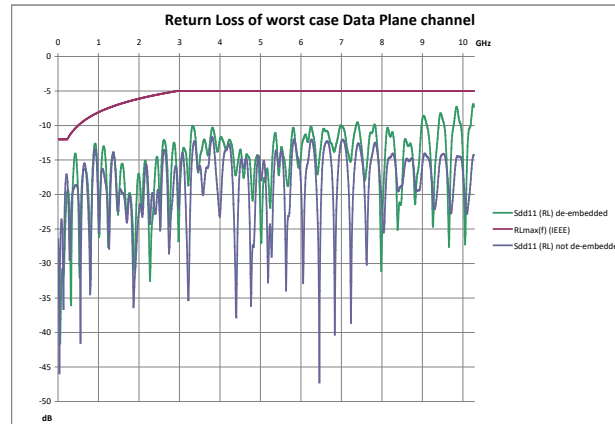
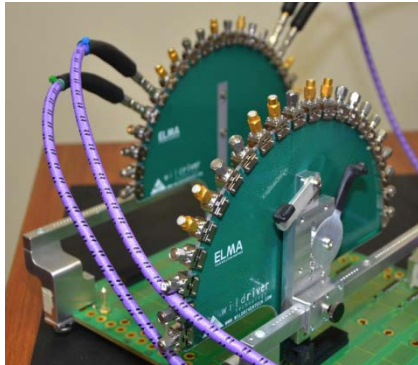
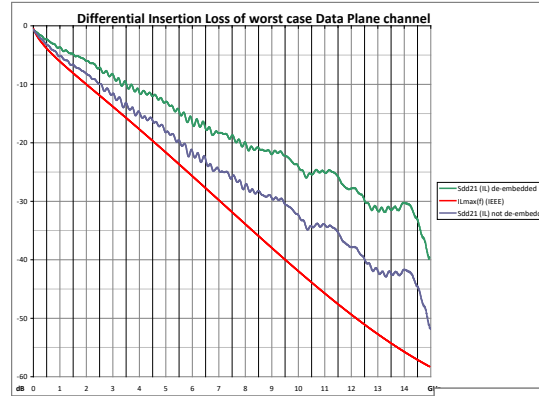
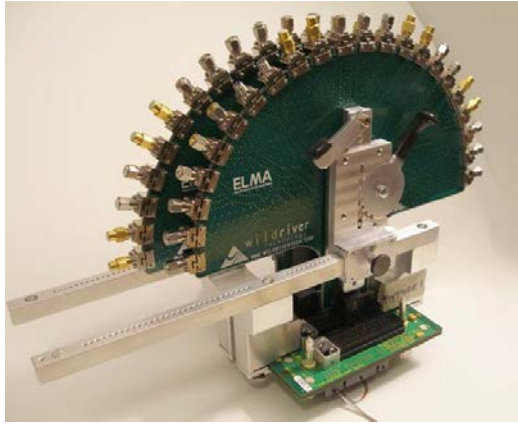
Scope is to measure the channel in the finished product. For practical reasons, this isn't always possible for a complex channel. Probe cards, micro-probing, or other types of fixturing can be used for extraction of S-parameters or time domain data.

Scope is to estimate how much of a difference there is between simulations and measurements and understand where the differences come from (and why).



Backplane channel measurements

Measurements and why good launches are necessary

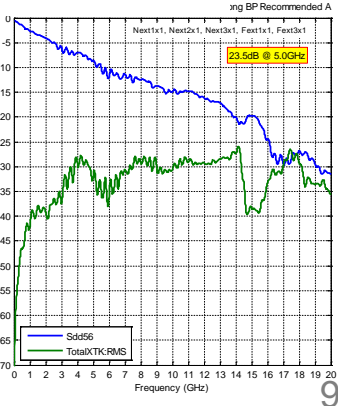
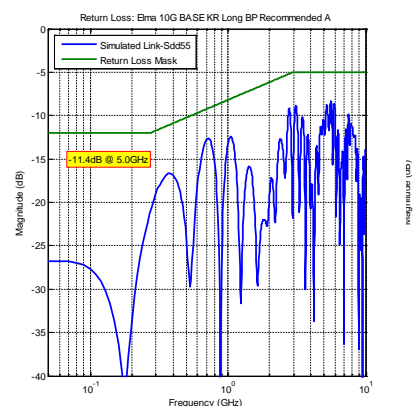
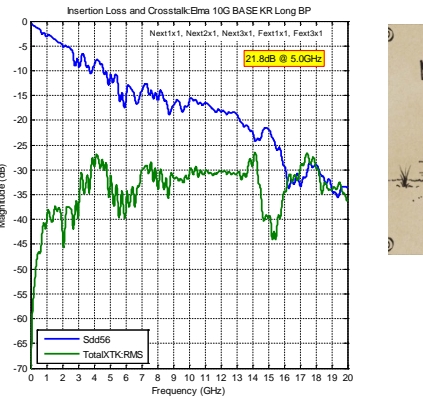
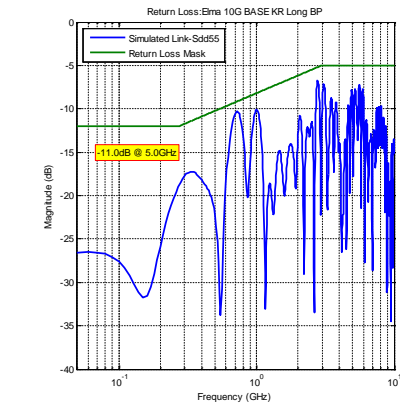
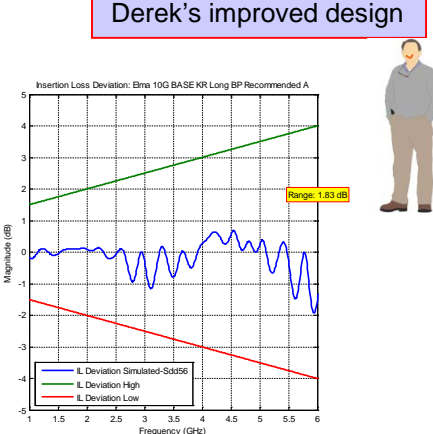
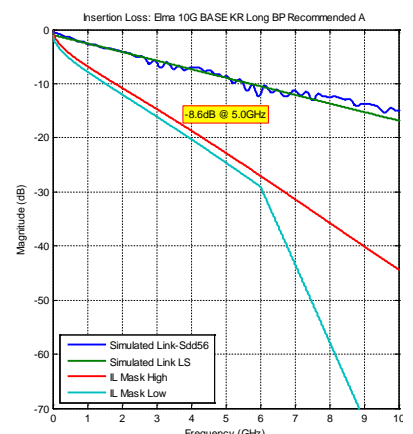
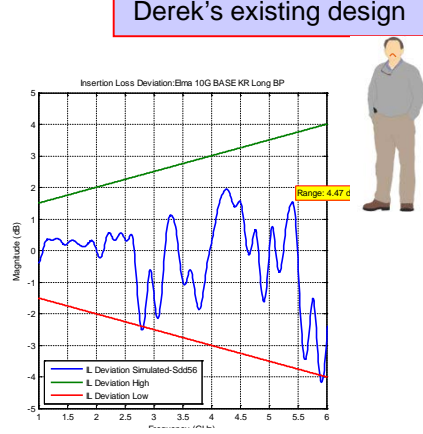
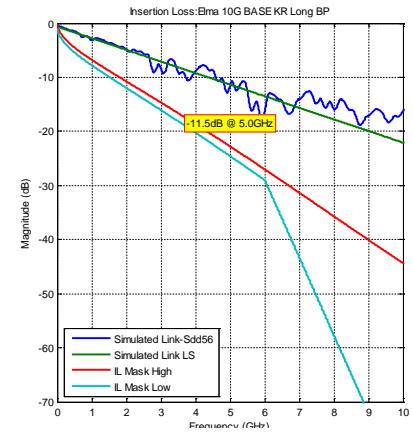


Channel co-design (& co-simulation!)

(or “Why Nancy, Alan, Derek, Chris & Ovidiu shouldn’t have a Mexican standoff”)

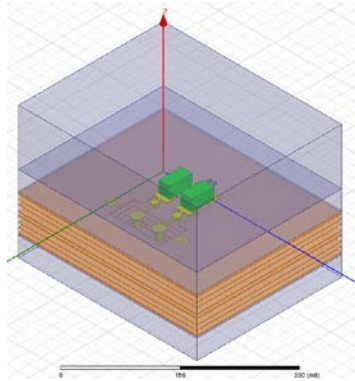
Derek's existing design

Derek's improved design

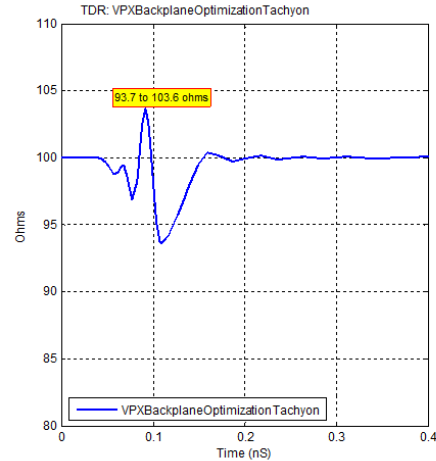
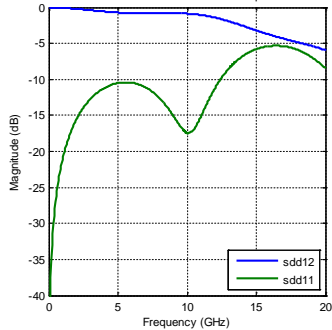


Channel co-design

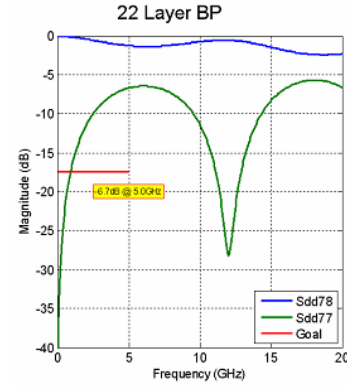
Improvements – vias on daughtercards and backplane



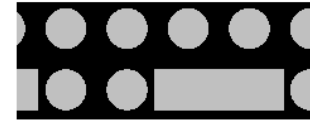
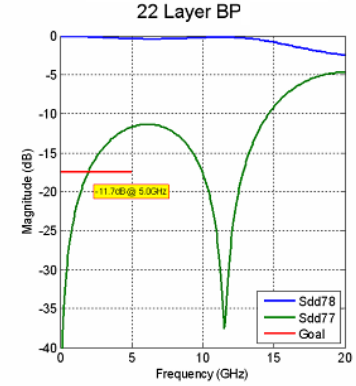
Differential Insertion and Return Loss: New Backplane RT-2 Via Model



VPX With round anti-pad on each pin

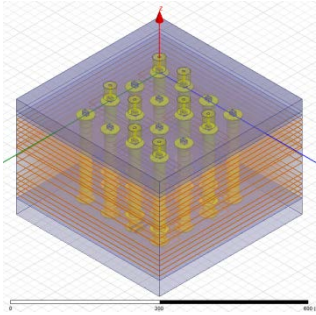


VPX With rectangular anti-pad

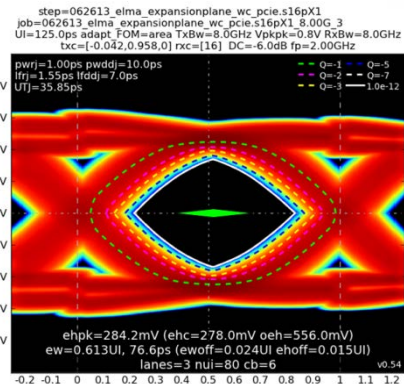
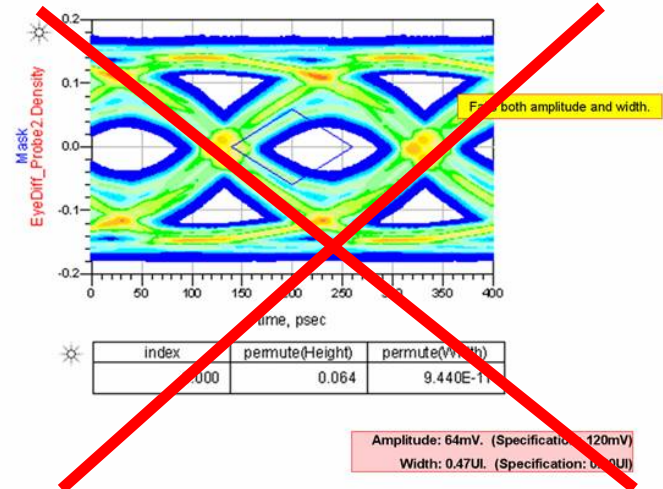
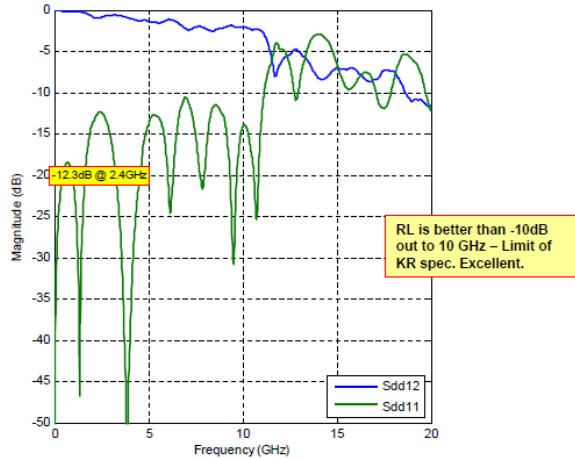


Channel co-design

Improvements for a common goal



Differential Insertion and Return Loss: VPXBackplaneOptimizationTachyon_onn_vias



- **Questions?**
- **Thank you for your time!**

- Ovidiu Mesesan
- Embedded Tech Trends 2018 Austin, Texas